



(19)

(11) Publication number:

**62004351 A**

Generated Document.

**PATENT ABSTRACTS OF JAPAN**(21) Application number: **60143734**(51) Int'l. Cl.: **H01L 23/48**(22) Application date: **29.06.85**

(30) Priority:

(43) Date of application publication: **10.01.87**(71) Applicant: **TOSHIBA CORP**

(84) Designated contracting states:

(72) Inventor: **SAITO TAMIO**

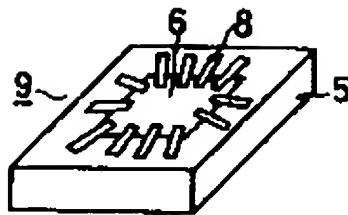
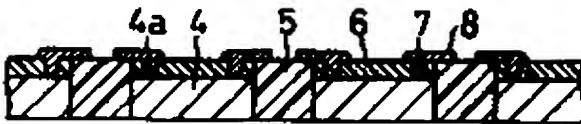
(74) Representative:

**(54) MANUFACTURE OF SEMICONDUCTOR CARRIER**

(57) Abstract:

**PURPOSE:** To improve the productivity, by burying a semiconductor chip in a package consisting of side members provided by insulator frames and of an upper member provided by an insulation layer, and by connecting an electrode pad on the chip to input/output terminals of a carrier through a conductor pattern.

**CONSTITUTION:** A semiconductor wafer 1 is cut off on a flexible support sheet 3 into separate chips 4. Insulator frames 5, which will be side members of a semiconductor carrier, are mounted in the gaps defined between the chips 4 so as to fill the gaps and to fix the chips positionally. An insulation layer 6, which will be a surface member, is then deposited on the chip. The insulation layer 6 is melt selectively above an electrode pad 4a on the chip 4 so as to provide an opening 7. Conductor patterns 8 are then formed on the surfaces of the insulator frames 5 and insulation layer 6 such that they are connected to the electrode pad 4a of the semiconductor chip through the opening 7 formed in the insulating layer 6. Finally, the insulator frame 5 is cut off between the



62004351 A

semiconductor chips 4 so that  
semiconductor carriers 9 each consisting of  
one chip are obtained.

COPYRIGHT: (C)1987,JPO&Japio